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Quick Tips

- Enter your search terms in lower case with a space between the terms.

      sales offices

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- Capitalize proper nouns to search for specific people, places, or products.

      John Colter, Netscape Navigator

- Enclose a phrase in double quotes to search for that exact phrase.

      "museum of natural history" "museum of modern art"

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      museum +art

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      museum -Paris

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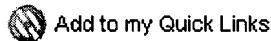   museum +"natural history" dinosaur -Chicago

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Term(s):
```
signal* w/15 wire* and wire* w/20 spare* and fault and
(emulat! or simulat!)
```

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Web   Results **1 - 10** of about **225,000** for <u>wires **signal** **spare** emulation **simulation** fault</u>. (**0.13** seconds)

Method and apparatus for the automatic correction of faulty **wires** ...
The logic **simulation** hardware **emulator** of claim 5, wherein the **spare** select .... Upon
detection of a **fault** on a regular **signal wire**, the runtime control ...
www.freepatentsonline.com/20050171756.html - 49k - <u>Cached</u> - <u>Similar pages</u>

Fault simulation system and a method for **fault simulation** - Patent ...
1 illustrates a **fault simulation** system, according to an embodiment of the invention; [0014]
FIG. 2 illustrates a front panel of a **signal** generator, ...
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Method and apparatus for processing an output of a design tool ...
Method and system for generating electronic hardware **simulation** models ... selecting
separate information relating to each **signal** in the selected part of ...
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Method and apparatus for processing an output of a design tool ...
Method and system for generating electronic hardware **simulation** models ... Information
relating to each **signal** in the selected part of the **signal** is then ...
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[PDF] An integrated diagnostic reconfiguration (IDR) technique for **fault** ...
Technique for **Fault** Tolerant Mixed **Signal**. Micros ys terns. Erfaan Sharif, Tony Dorey ....
the **simulation** results from stage 4. The reconfiguration ...
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[PDF] BIST-based delay-**fault** testing in FPGAs - On-Line Testing Workshop ...
require either ATPG or **fault simulation**, which are computa-. tionally expensive tasks for
ASICs .... A **signal** path is formed by connecting several **wire** seg- ...
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hardware interface functions to. unmapped memory and handle the resulting page **faults**
by. **emulating** the 1/0 instruction. with co-**simulation** ...
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[PDF] BIST-Based Delay-**Fault** Testing in FPGAs
tern Generation (ATPG) or **fault simulation**, which are. computationally expensive tasks
for ... **signal** paths. Similarly, for interconnect test, the **wires** ...
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Chip Design Made Easy - Wikibooks, collection of open-content ...
Step 16: Perform the Package **wire**-bonding, which connects the chip to the ..... **Simulation**
Thermal **Simulation** Noise **Simulation** Test **Simulation** Emulation ...
en.wikibooks.org/wiki/Chip_Design_Made_Easy - 52k - <u>Cached</u> - <u>Similar pages</u>

[PDF] BIST-Based Delay **Fault** Testing in FPGAs
File Format: PDF/Adobe Acrobat - <u>View as HTML</u>
A **signal** path is formed by connecting several **wire** ..... We have **emulated** many delay-

faults by creating a "faulty" PUT longer than the other "**fault**-free" ...
www.eng.auburn.edu/users/strouce/class/bist/jetta03.pdf - <u>Similar pages</u>

1 <u>2</u> <u>3</u> <u>4</u> <u>5</u> <u>6</u> <u>7</u> <u>8</u> <u>9</u> <u>10</u>   **<u>Next</u>**

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| wires signal spare emulation simulat | **Search** |

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☐	L3	((signal? with wire?) with spare) and fault and (emulat$ or simulat$).clm.	1
☐	L2	((signal? with wire?) with spare) and fault and (emulat$ or simulat$) and (703/13,14,23-28.ccls. or 370/216-228,352.ccls. or 714/25-31.ccls.)	1
☐	L1	gooding.in. and (((signal? with wire?) with spare) same fault) and (emulat$ or simulat$)	0

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